

Heller Ehrman LLP
Title: "METHOD AND APPARATUS FOR SELFREFERENCED WAFER STAGE POSITIONAL ERROR
MAPPING"
Inventor(s): A. Smith et al.
Application No.: 10/775,718 – Filed: 02/09/2004
Atty Docket No.: 38203-6082B
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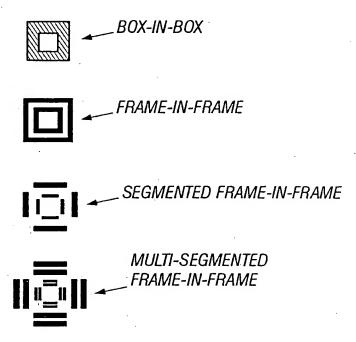


FIG. 1

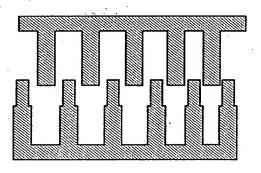
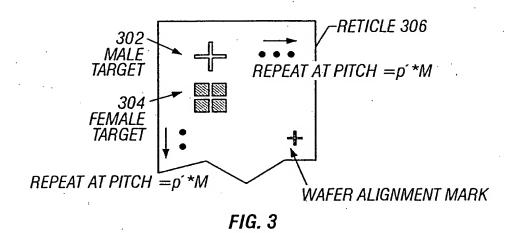
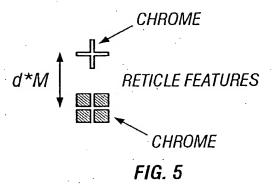


FIG. 2

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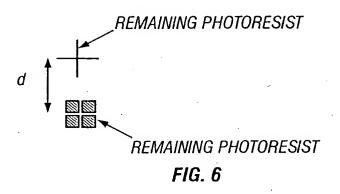


FIG. 7

um=microns, Dark=unexposed, white=exposed.

1 20um x 20um

FIG. 8A

um=microns, Dark=chrome, white=clear.

FIG. 8B

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FIG. 9

um=microns, Dark=unexposed, white=exposed.

FIG. 10A

um=microns, Dark=chrome, white=clear.

200um 1 40um x 40um

FIG. 10B

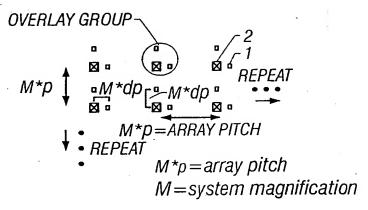


FIG. 11

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(3 featured parts); dark=unexposed, white=exposed.

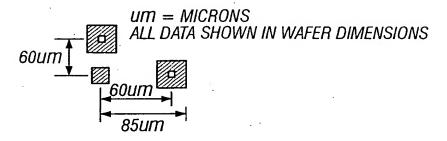


FIG. 12A

dark=unexposed, white=exposed. um=microns at wafer.

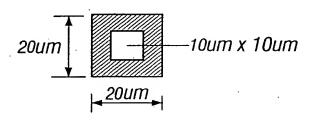
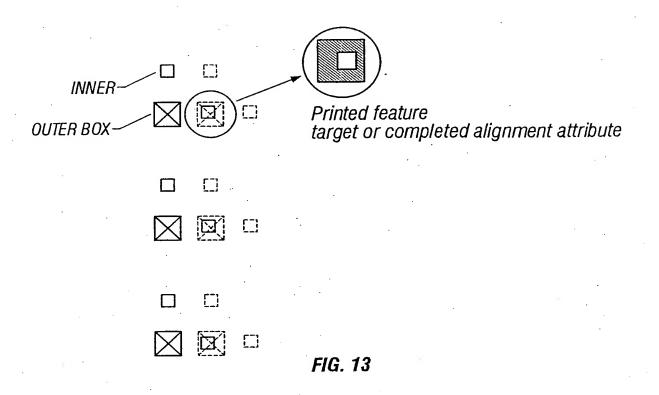


FIG. 12B

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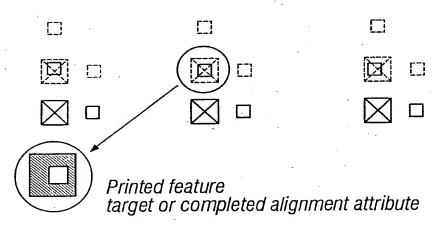


FIG. 14A

Inventor(s): A. Smith et al.

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CA = completed alignment attribute, UA = unusable alignment attribute

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FIG. 14B

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Title: "METHOD AND APPARATUS FOR SELFREFERENCED WAFER STAGE POSITIONAL ERROR
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8/23 PROVIDE INTRA-FIELD DISTORTION. COMPUTE STAGE ERRORS. COMPUTE STAGE ERRORS. PROVIDE INTRA-FIELD DISTORTION. PROVIDE INTRA-FIELD DISTORTION COMPUTE STAGE ERRORS. DEVELOP WAFER AND MEASURE OVERLAY TARGETS DEVELOP WAFER AND MEASURE OVERLAY TARGETS DEVELOP WAFER AND MEASURE OVERLAY TARGETS REPEAT INTERLOCKING SUB-Eo exposures nymes REPEAT INTERLOCKING SUB-EO EXPOSURES IN TIMES FIG. 16 FIG. 17 FIG. 15 INTERLOCKING PATTERN ON WAFER **EXPOSE RETICLE IN** EXPOSE WAFER AT SUB

E0 DOSE IN INTERLOCKING

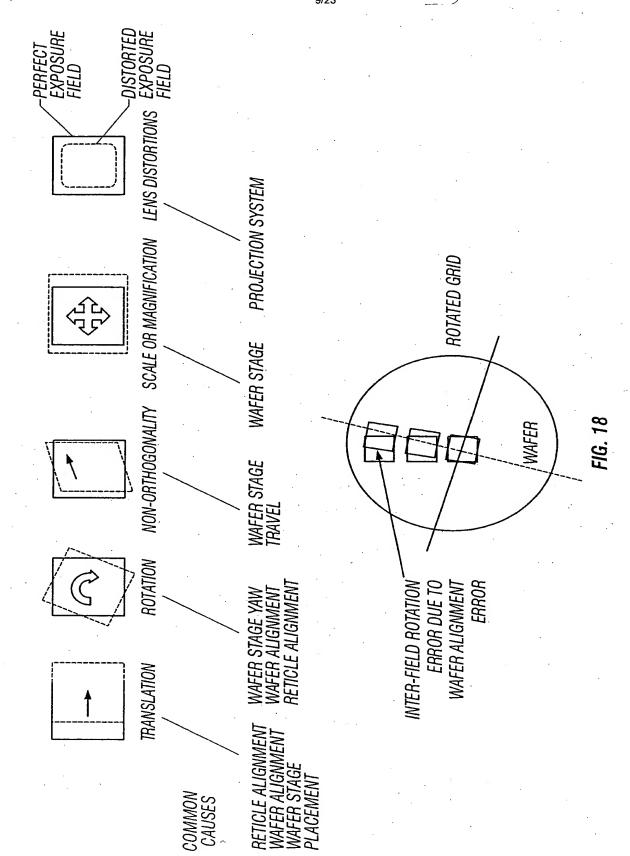
PATTERN ON WAFER EXPOSE WAFER AT SUB
EO DOSE IN INTERLOCKING
PATTERN ON WAFER LOAD AND ALIGN RETICLE PROVIDE RETICLE. OAD AND ALIGN RETICLE PROVIDE RETICLE WITH DECREASED OPTICAL TRANSMISSION. LOAD AND ALIGN RETICLE PROVIDE RETICLE

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RETICLE AND WAFER STAGE

FIG. 19

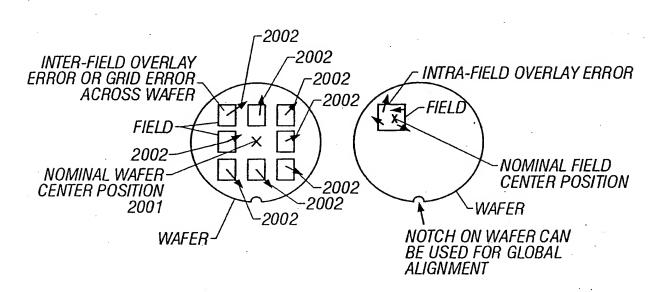


FIG. 20A

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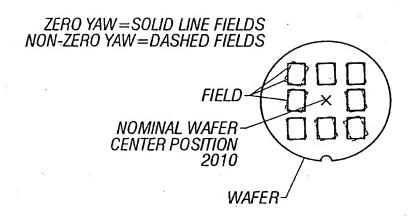


FIG. 20B

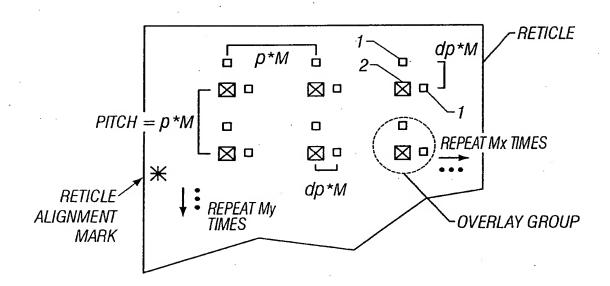


FIG. 21A

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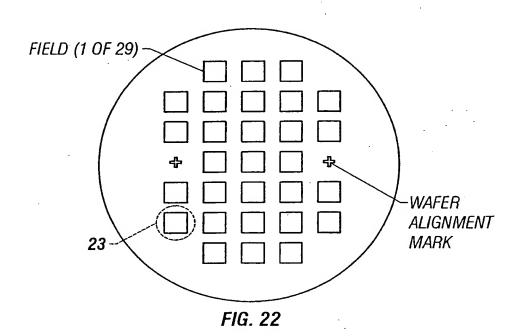
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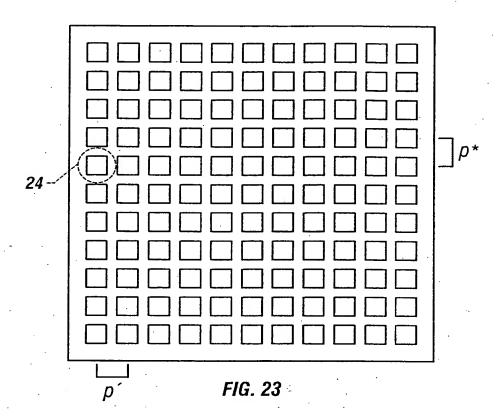
-TOP, POSSIBLY COATED FOR REDUCED TRANSMISSION

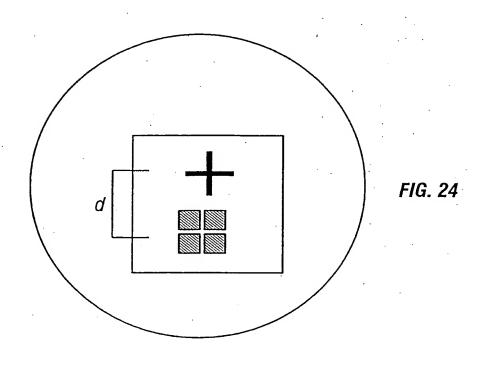
-CHROME SURFACE (BOTTOM), POSSIBLE COATED FOR REDUCED TRANSMISSION

FIG. 21B



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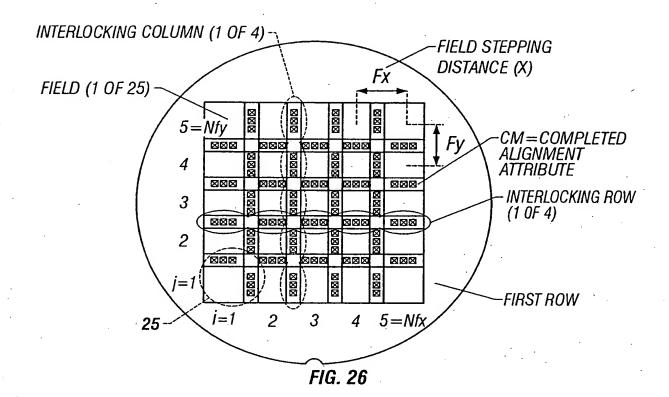


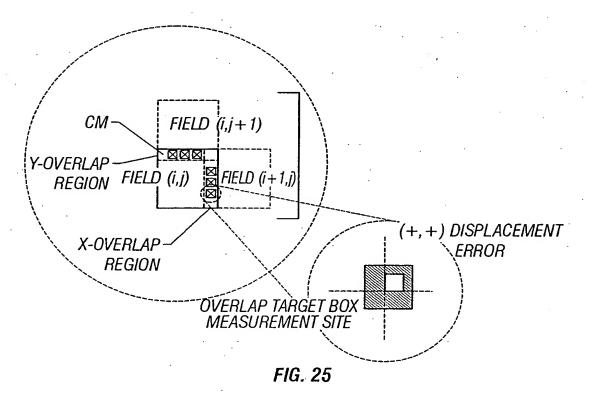


Inventor(s): A. Smith et al.

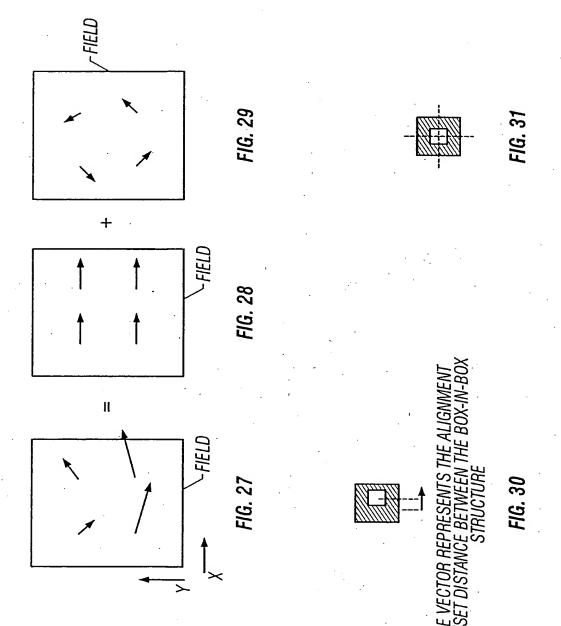
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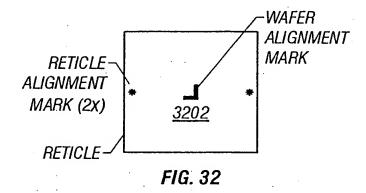


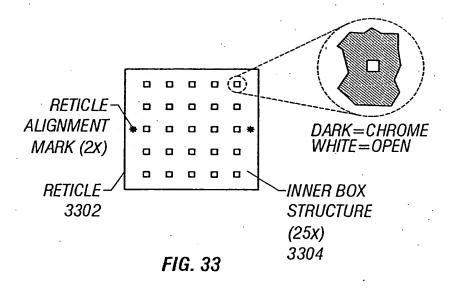
Inventor(s): A. Smith et al.

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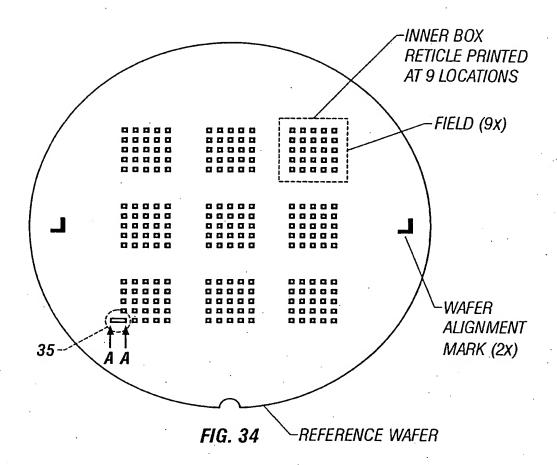


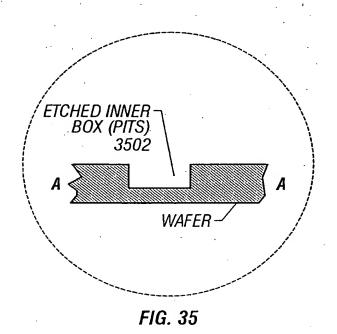


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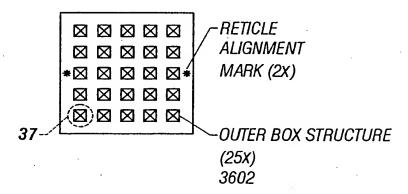


FIG. 36

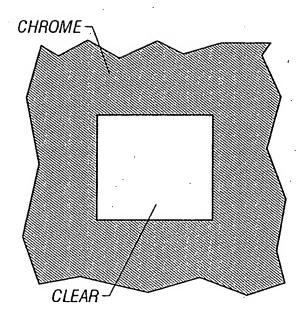
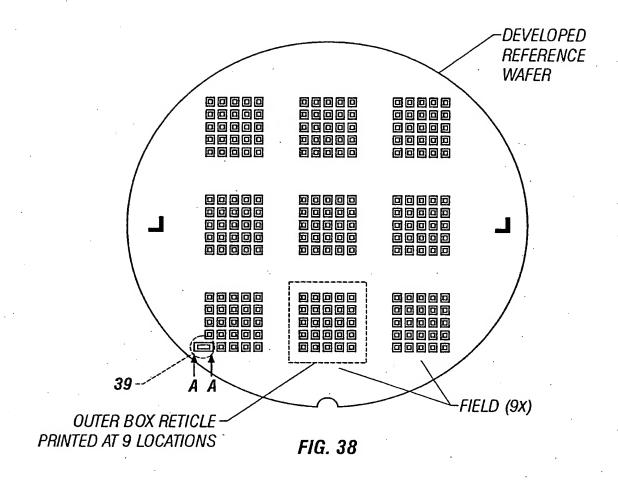


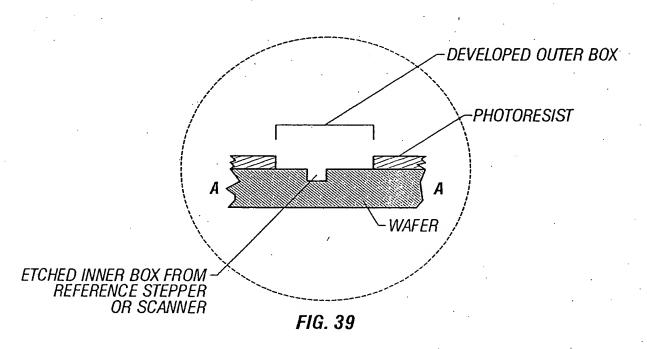
FIG. 37

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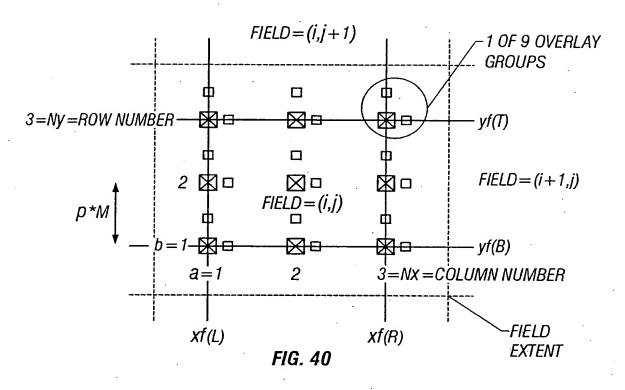
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Dark=chrome, white=clear.

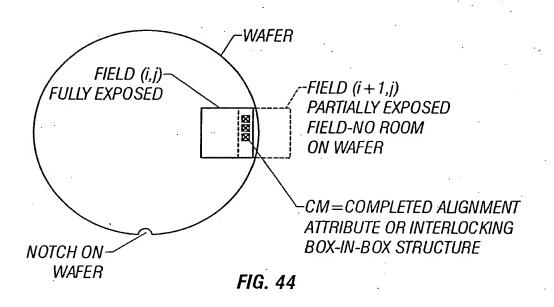
Dark=chrome, white=clear.



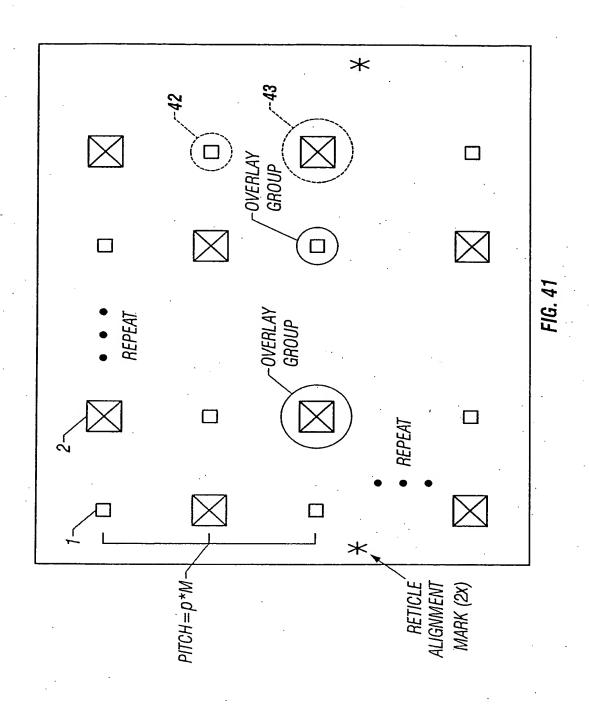
FIG. 42



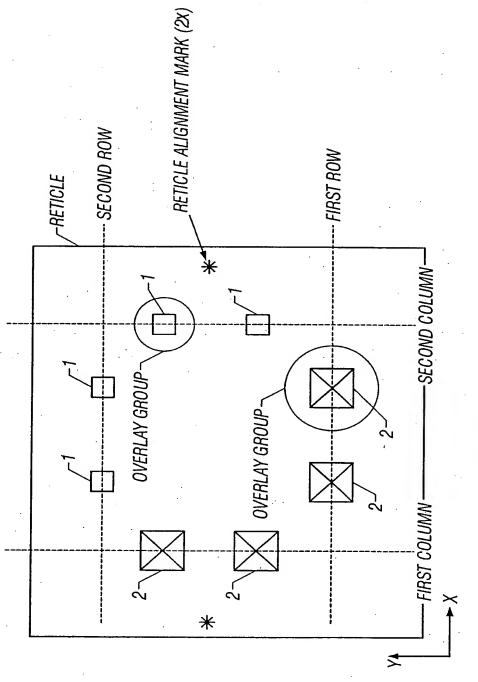
FIG. 43



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Inventor(s): A. Smith et al.
Application No.: 10/775,718 – Filed: 02/09/2004
Atty Docket No.: 38203-6082B

Length units = microns,
Yaw units = microradians,
xG, yG = nominal field center position.
dxG, dyG = offset of center of field.
Qg = yaw of field.
Fx, Fy = field stepping distance,
srel = grid scale - intra-field scale (parts per million),
D = wafer diameter.

Fx : 200 Fy : 200	7X5J 000.000 000.000 000.000 -39.455			
xG -100000.000 -80000.000 -60000.000	уG 0.000 0.000 0.000	dxG -0.139 0.223 0.498	dyG 0.044 -0.233 0.004	Qg 10.3 94.0 -34.7
60000.000		0.099	-0.188	59.2

FIG. 46